Lokmanya Tilak Jankalyan Shikshan Sanstha's
PRIYADARSHINI COLLEGE OF ENGINEERING
(Recognised by A.I.C.T.E., New Delhi & Govt. of Maharashtra, Affiliated to R.T.M.Nagpur University)
Near CRPF Campus, Hingna Road, Nagpur-440 019, Maharashtra (India)
Phone : 07104 – 236381, 237307, Fax : 07104 – 237681,
email : principal.pce.ngp@gmail.com, www.pcenagpur.edu.in

6.5.3 Quality assurance initiatives of the institution include:

1. Regular meeting of Internal Quality Assurance Cell (IQAC); Feedback collected, analyzed and used for improvements
2. Collaborative quality initiatives with other institution(s)
3. Participation in NIRF
4. Any other quality audit recognized by state, national or international agencies (ISO Certification, NBA)

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1. NAAC: "One day National Webinar on NAAC Assessment Guidelines in Post Covid-19 Era"

Lokmanya Tilak Jankalyan Shikshan Sanstha's
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Lokmanya Tilak Jankalyan Shikshan Sanstha's

PRIYADARSHINI COLLEGE OF ENGINEERING

Priyadarshini Campus, Digdoh Hills, Hingna Road, Nagpur-440019

Invites You

TO INAUGURAL FUNCTION OF

ONE DAY NATIONAL WEBINAR

On

NAAC ASSESSMENT AND ACCREDITATION GUIDELINES IN POST COVID-19 ERA

organised by

INTERNAL QUALITY ASSURANCE CELL

In association with

NATIONAL ASSESSMENT AND ACCREDITATION COUNCIL (NAAC)

Function will be presided by

Dr. Ganesh Hegde
Advisor, NAAC

Dr. Leena Gahane, Dy. Advisor, NAAC

Dr. A.V.Prasad, Asst. Advisor, NAAC

Dr. N.R.Mohan, Asst. Advisor, NAAC

In presence of

Dr. M.P. Singh,
Principal

Dr. S.A. Dhale,
Vice Principal

30th September 2020 from 11:00 am

Dr. (Mrs.) A.P Rathkanthiwar,
NAAC Coordinator

Dr.(Mrs.) S.W.Varade
Co-convener

Dr.S.S. Shriramwar,
Convener & IQAC Coordinator

Lokmanya Tilak Jankalyan Shikshan Sanstha's
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INTERNAL QUALITY ASSURANCE CELL

In association with

NATIONAL ASSESSMENT AND ACCREDITATION COUNCIL (NAAC)

Organizes

ONE DAY NATIONAL WEBINAR

On

NAAC ASSESSMENT AND ACCREDITATION GUIDELINES IN POST COVID-19 ERA

Organized by : Internal Quality Assurance Cell in association with in association with National Assessment & Accreditation Council (NAAC), Bangalore.

No. of registrations : 541

Participated by : 376 Participants from different parts of the country .

Mode of Conduction: Cisco WebEx & Live streaming on You tube.

Date: 30th September 2020

Event: One day National Webinar on NAAC Assessment & Accreditation Guidelines in Post COVID-19 Era

Objective: To create awareness & to discuss the new online process about NAAC Accreditation and its benefits to the higher education Institutions for quality enhancement.

Resource Persons:

Dr. Ganesh Hegde : Advisor, NAAC

Dr. Leena Gahane : Deputy Advisor, NAAC

Dr. A. V. Prasad : Assistant Advisor, NAAC

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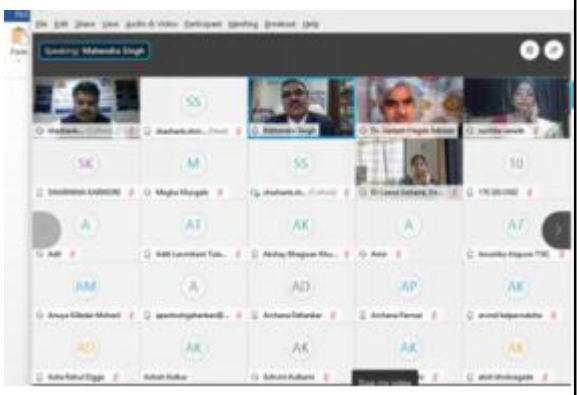
email : principal.pce.ngp@gmail.com, www.pcenagpur.edu.in

Coordinators:

Dr.M.P.Singh	Chairperson
Dr.S.S.Shriramwar	Convener, IQAC Coordinator
Dr.(Mrs.)S.W.Varade	Co-Convener
Dr.Mrs.A.P.Rathkanthiwar	Coordinator
Dr.(Ms.)R.A.Keswani	
Mr.Punesh Tembhare	
Mr.A.Nilewar	Organizing Team
Ms.S.G.Mungale	

Remark: Participants were enriched with the informative and thought provoking sessions shared by he NAAC team. NAAC Team clarified the doubts raised by the participants and agreed to support the Institutions on all accreditation clarifications through their Help Desk and other supportive interventions.



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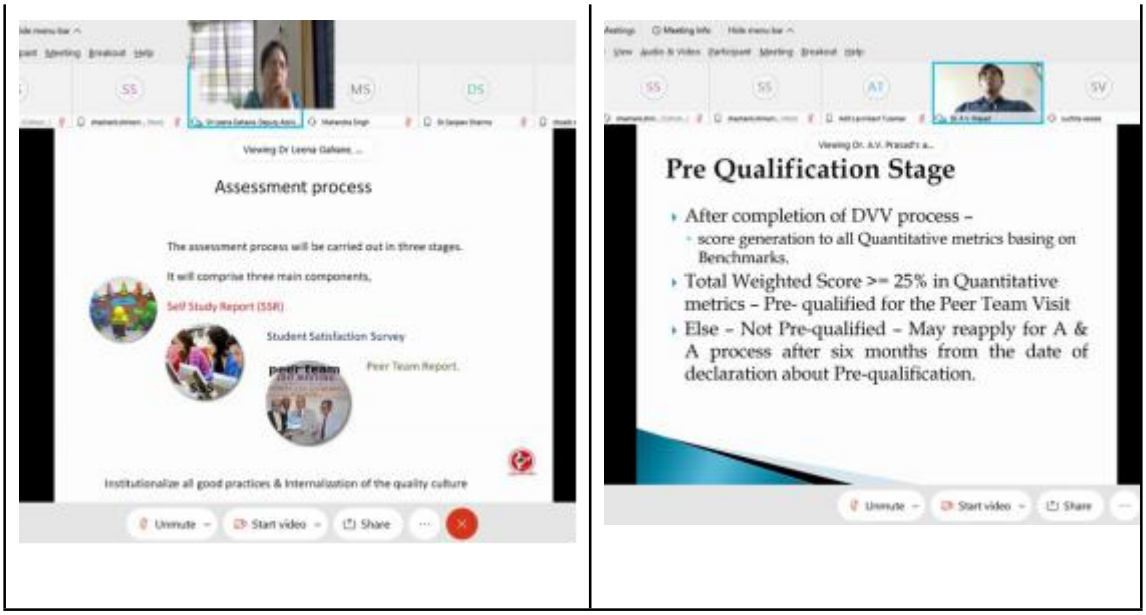

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2. AICTE STTP on "Recent Trends and Applications of Wireless Communication in VLSI Design"

REGISTRATION FORM

AICTE Sponsored
One Week Online Short Term Training Program (STTP)
On

Recent Trends & Applications of Wireless Communication in VLSI Design

22nd to 27th March 2021

Registration form Link
https://forms.gle/KHUBWwRQhKpoBZBY9

Name: _____

Designation: _____

Qualification: _____

Department: _____

College/Organization: _____

Contact Address: _____

_____

_____

Mobile Number: _____

E-mail: _____

Date: Signature of Applicant

Name/ Signature of Head of Institution

Kindly email this form at
awani.gaidhane@gmail.com

Chief Patrons
Dr. Satish Chaturvedi, Chairman, LTJSS, Nagpur.
Smt. Abha Chaturvedi, Secretary, LTJSS, Nagpur

Patrons
Shri. Dushyant Chaturvedi, Director (GB), LTJSS
Smt. Sheetal Chaturvedi, Member (GB), LTJSS
Shri. Abhijeet Deshmukh, Director, LTJSS

STTP chairperson
Dr. M.P. Singh, Principal, PCE

Advisory Board
Dr. S.A. Dhale, Vice Principal, PCE
Dr.K.S. Zakiuddin ,Asso. Dean (R&D), PCE
Dr.P.R.Rothe. Dean, SW&C, PCE
Dr.Mrs. S.W.Varade, Professor, Dept of E &TC
Dr. V.K.Taksande, HOD Dept of E&TC.

Convener
Dr.S.S.Shriramwar, Professor & Dean Academics

Coordinator
Dr. (Mrs.).A.S.Khobragade
Prof. (Ms.) S. G.Mungale

Organising Committee
Prof. (Mrs.) P.J.Suryawanshi
Prof. C.N. Bhoyar
Prof. (Mrs.) A.P.Khandait.
Dr. (Mrs.) M.V. Vyawahare
Prof. (Ms.) D. Meshram
Prof. (Mrs.) K.M.Bogawar
Prof. R.C. Iyer

Lokmanya Tilak Jankalyan Shikshan Sanstha's
PRIYADARSHINI COLLEGE OF ENGINEERING
NAGPUR (MAHARASHTRA)

AICTE Sponsored

One Week Online Short Term Training Program (STTP)
On

Recent Trends & Applications of Wireless Communication in VLSI Design

22nd to 27th March 2021

ORGANIZED BY

Internal Quality Assurance Cell
&
Department of Electronics Engineering

Priyadarshini College of Engineering

Priyadarshini Campus, Hingna Road ,Nagpur-440019
07104-244681
www.pcenagpur.edu.in
Affiliated to RTM Nagpur University
NAAC Accredited with A+ grade

Lokmanya Tilak Jankalyan Shikshan Sanstha's

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Priyadarshini College of Engineering

Priyadarshini Campus, Hingna Road Nagpur-440019
www.pcenagpur.edu.in

Affiliated to RTM Nagpur University

Internal Quality Assurance Cell

AICTE Sponsored

Online Short Term Training Program (STTP)

On

Recent Trends & Applications of wireless communication in VLSI Design

22nd to 27th March 2021

Organized by : Internal Quality Assurance Cell & Department of Electronics Engineering.

Participated by : Research Scholars, Academicians from Electronics background across the country.

Mode of Conduction: Google Meet

Date: 22nd March- 27th March 2021

Event: AICTE sponsored One Week Online Short Term Training Program On Recent Trends & Applications of Wireless Communication in VLSI Design.

Objectives: To recognize the role of VLSI Design in wireless communication system.

To discuss the hardware design issues for next generation wireless communication system using VLSI.

Insights about technological details of VLSI Circuits.

To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in Wireless Communication using VLSI system design.

To provide scope for Applied Research and innovation in the various fields of VLSI.

To explore new development & innovations & possibility of research in the recent trends in Wireless communication.

Resource Persons:

Day/Date	Time	Speaker	Topic
Day 1 22/03/21 Monday	11:30 to 11:45 am	Inauguration	
	11:45 am to 1:00 pm	Prof. Mukul S. Sutaone Deputy Director College of Engineering, Pune	Evolution of Telecommunication Network : 1G to 5G

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	1:00 to 2:30 pm	Dr.R.D.Raut, Associate Professor, Govt.College of Engineering Nagpur	Cognitive Radio Communication & SDR design
Day 2 23/03/21 Tuesday	2:00 to 3:00 pm	Dr.Surendra Singh Rathod, Professor, Sardar Patel Institute of Technology, Mumbai	Fundamentals of Data Converters.
	3:00 to 5:00 pm	Dr.Prabhat Sharma Assistant Professor, VNIT, Nagpur	Wireless Communication using Python: Theory & Hands on.
Day 3 24/03/21 Wednesday	2:00 to 3:00 pm	Mr.H.S.Jatana Divisional Head, Semi-Conductor Laboratory / ISRO , Mohali	Recent trends in Semiconductor Chip Design
	3:00 to 5:00 pm	Mr.Oveek Chatterjee Founder Elentrika Technologies & Technical Head Lets Author Technologies, Nagpur	Introduction & Basics of GNU Radio Programming Environment
Day 4 25/03/21 Thursday	2:00 to 3:00 pm	Mr.Lochan Keote Asst.General Manager,BSNL Nagpur	Wimax, VSAT, HAM Radio design challenges.
	3:00 to 4:00 pm	Mr.Sai Krishna D. Tirmanwar Design Engineer, Moschip Technologies, Hyderabad	IC design on cadence Virtuoso.
	4:00 to 5:00 pm	Mr.Debanjan Kundu & Mr.Shubham Thakre Intel Technology India Pvt Ltd. Banglore	ASIC Design Flow
Day 5 26/03/21 Friday	2:00 to 3:00 pm	Dr.Sheetal Gundal, Associate Professor & HOD Electronics Engineering Amrutvahini College of Engineering, Sangamner	Speech coder for Software Defined Radio : FPGA Implementation
	3:00 to 5:00 pm	Mr. Ashish khachane Senior Engineer Field Application - Xilinx Excel point System Ltd, Bangalore	Design and Development of 5G Radio Units and Baseband Discrete Units for Sub –Six GigaHertz Bands.
Day 6 27/03/21 Saturday	2:00 to 4:00 pm	Mr. Nirmesh Kumar Awasthi, Senior Staff Engineer , ST Microelectronics, Gr. Noida	High Speed I/O design for Wireless Communication.
	4.00 pm	Valedictory Function	

Coordinators:

Dr.M.P.Singh	Chairperson
Dr.S.S.Shriramwar	Convener STTP, IQAC Coordinator
Dr.Mrs.A.S.Khobragade	Coordinator-STTP
Ms.S.G.Mungale	Coordinator-STTP
Mr.R.C.Iyer	Coordinator-STTP

Remark: Participants were enriched with the knowledge shared by expert speakers to keep pace with the changing scenario in the field of Wireless Communication.

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3. AICTE STTP on "Recent Trends and Applications on Digital VLSI Design"

REGISTRATION FORM

AICTE Sponsored
One Week Online Short Term Training Program (STTP)
On
Recent Trends & Applications in Digital VLSI Design
14th to 19th December 2020

Registration form Link
https://forms.gle/SmsSrj1DnmyeaTGb8

Name: _____
Designation: _____
Qualification: _____
Department: _____
College/Organization: _____
Contact Address: _____
_____
_____
Mobile Number: _____
E-mail: _____

Date: Signature of Applicant

Name/ Signature of
Head of Institution

Kindly upload this form on registration link

Chief Patrons
Dr. Satish Chaturvedi, Chairman, LTJSS, Nagpur.
Smt. Abha Chaturvedi, Secretary, LTJSS, Nagpur

Patrons
Shri. Dushyant Chaturvedi, Director (GB), LTJSS Nagpur
Smt. Sheetal Chaturvedi, Member (GB), LTJSS, Nagpur
Shri. Abhijeet Deshmukh, Director, LTJSS, Nagpur

STTP chairperson
Dr. M.P. Singh, Principal, PCE

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Dr.P.R.Rothe. Dean, SW&C, PCE
Dr.Mrs. S.W.Varade, Professor,Dept of E &TC
Dr. V.K.Taksande, HOD Dept of E&TC.

Convener
Dr.S.S.Shriramwar, Professor & Dean Academics,PCE

Coordinators
Dr. (Mrs.)M.V.Vyawahare
Prof. (Mrs.) A.P.Khandait.
Prof (Mrs.) D.Meshram

Organising Committee
Prof. (Mrs.) P.J.Suryawanshi
Prof. C.N.Bhoyar
Prof.(Ms.) S.G.Mungale
Prof.(Mrs.) K.M.Bogawar
Dr.(Mrs).A.S.Khobragade
Prof. R.C. Iyer

Lokmanya Tilak Jankalyan Shikshan Sanstha's
PRIYADARSHINI COLLEGE OF ENGINEERING
NAGPUR (MAHARASHTRA)

AICTE Sponsored
One Week Online Short Term Training Program (STTP)
On

Recent Trends & Applications in Digital VLSI Design

14th to 19th December 2020

ORGANIZED BY
Internal Quality Assurance Cell
&
Department of Electronics Engineering
Priyadarshini College of Engineering
Priyadarshini Campus, Hingna Road Nagpur-440019
07104-244681
www.pcenagpur.edu.in
Affiliated to RTM Nagpur University
NAAC Accredited with A+ grade
Platinum Category in AICTE-CII Survey

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About Institute

Priyadarshini College of Engineering, Nagpur the Premier College of the LTJSS Spread over a sprawling 72 acres,the campus is enriched with state of the art sports and recreational facilities. The Institute has a 32 years of Proven Track Record, endeavors to impart Academic Excellence through promoting technology, scientific thinking and Corporate Social Responsibility. Priyadarshini College of Engineering has been **awarded with A+ grade status with CGPA 3.31 by NAAC** for a term of 5 years up to 27.03.2024.The **institute has received accreditation for three of its programs**, namely Civil Engineering, Mechanical Engineering, and Electrical Engineering up to 30/06/2021 by **National Board of Accreditation (NBA)**, New Delhi. The Institute runs **7 undergraduate programs, 4 post Graduate Programs and 3 Ph.D. Programs. Institute has a strong faculty pool with 50 Ph.D. awarded and 32 ongoing.** The Institute has also been conferred with **Grade A** by the Government of Maharashtra for Academic Excellence and is the recipient of **Platinum Rank Category in AICTE-CII survey in 2019**.The Institute has also **received World Education Award**, India's Education Excellence Award 2018, Berkshire Media USA; and **Outstanding Engineering Institute** for Research and Innovation held at 15th World Education Summit-2019.

About STTP

Due to the rapid growth and advancement of the Very Large Scale Integration (VLSI), the Electronics Industries have achieved tremendous growth from last few years.
VLSI technology has opened vast opportunities for career growth in design implementations, verification, computer-aided designing, testing and simulation. So there is a need to produce highly skilled design engineers. The aim of this course is to upgrade the information about the recent trends & applications in Design of Digital VLSI circuits. Exposure and hands-on training with VLSI Design tools will be part of the course. This STTP also aims to share the experiences of professionals working in the domain of Digital VLSI Design which will help the research scholars and the faculty members to get the indepth knowledge in the field of Digital VLSI design

STTP Objectives

- Recognize the role of Digital VLSI design in semiconductor industry & industrial challenges.
- Development of trained resources in VLSI design
- Interaction of the participants with the experts from academic institutes & Industry.
- Insights about technological details of Digital VLSI- a) Static MOS gate circuits, b) High-Speed CMOS Logic Design, c) Transfer Gate and Dynamic Logic Design

Resource Persons

Distinguished faculty members from the renowned Institutes like IIT, NITs, and experts from Industries and other leading Organizations (DRDO) will be delivering the Lectures/demonstrations.

Major Contents

- Introduction to VLSI and Industry Overview
- Digital VLSI- a) Static MOS gate circuits, b) High-Speed CMOS Logic Design, c) Transfer Gate and Dynamic Logic Design
- Invited talks delivered by experts from industry and Academic Organizations
- Demonstrations through simulations.

Expected Outcomes

- Participants will get an Insight with the experts from Academic Institutes & Industry on various tools.
- Participants will acquire knowledge and hands on experiences in VLSI design using state of the art EDA tools
- Exposure in the area of design of Front End and back end VLSI Design

Registration Guidelines

- Register on following link
  https://forms.gle/SmsSrj1DnmyeaTGb8
- Seats are limited and selection will be based on first come first serve basis. Kindly register before 10th December 2020.
- Confirmation email will be sent to the selected candidates.
- E-Certificate will be issued to the participants who attend all the sessions of the STTP and pass the Examination.
- **Registration Fees: Nil**

Contact

Dr. (Mrs.)M.V.Vyawahare 9420246938
Prof. (Mrs.) A.P.Khandait. 7219607656
Prof (Mrs.) D.Meshram 9421704683

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AICTE Sponsored

One Week Online Short Term Training Program (STTP)

On

Recent Trends & Applications in Digital VLSI Design

14th to 19st December 2020

Eminent Speakers

Mr.Prathipan.K
Research Scientist, DRDO

Dr.J.L. Mazher Iqbal
Professor, Veltech Rangarajan Dr.Sagunthala R&D institute of Science and Techlogy , AVADI Chennai

Dr. Surendra S. Rathod
Professor
Sardar Patel Institute of Technology, Mumbai

Dr.P.K. Dakhole
Professor & Registrar
YCCE, Nagpur

Dr.Mrs.A.A. Khurshid
Professor & Head(EN/EDT)
RKNEC , Nagpur

Pankaj Bande
Chief Technology Officer, Wizclub

Mr. Sachin Pampattiwar
Senior Staff Engineer
Qualcomm Technologies International Ltd

Mr.Ashish Khachane
Senior Engineer Field Application
Xilinx Excel point System Ltd,Banglore

Mr.Aalhad Deshpande
Marvell Semiconductor

Dr.Mrs. Anuja Askhedkar
Associate Professor
MIT ,WPU,Pune

Dr. Nitin Narkhede
Associate Professor
RKNEC, Nagpur

Organised By

Internal Quality Assurance Cell

&

Department Of Electronics Engineering

Priyadarshini College of Engineering ,Nagpur

Dr. Mrs.P. Palsodkar
Assistant Professor
YCCE, Nagpur

Dr.Sandeep Kakde
Assistant Professor
YCCE, Nagpur

Dr. M.P. Singh, Principal

Dr. S.A. Dhale, Vice Principal

Dr.S.S.Shriramwar, Convener

Dr(Mrs).M.V.Vyawahare, Coordinator
Mrs.A.P.Khandait, Coordinator
Ms. Divya Meshram,Coordinator

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Report on
AICTE Sponsored
One Week Online Short-Term Training Program (STTP)
On

Recent Trends & Applications in Digital VLSI Design

14th to 19th December 2020

AICTE sponsored Online One Week Short Term Training Program on Recent Trends & Applications in Digital VLSI Design was held by Internal Quality Assurance Cell (IQAC), & Department of Electronics Engineering, PCE from 14th -19th December 2020.
This STTP aimed to give exposure to Recent Trends & Applications in the area of Digital VLSI Design.

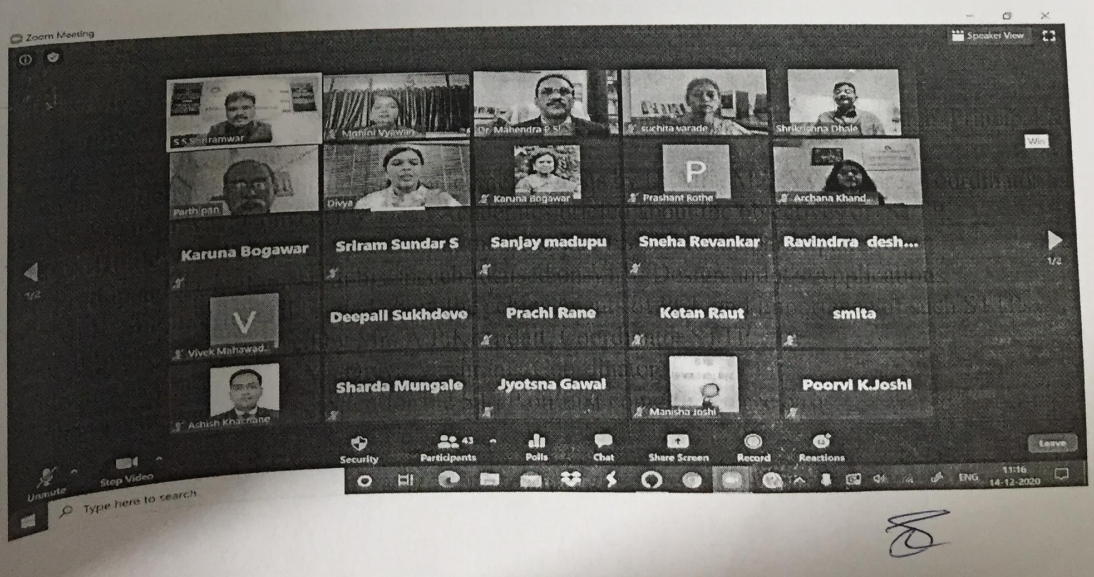
Objectives:

- To Recognize the role of Digital VLSI design in semiconductor industry & industrial challenges.
- For development of trained resources in VLSI design
- Interaction of the participants with the experts from academic institutes & Industry.
- To give Insights about technological details of Digital VLSI- a) Static MOS gate circuits, b) High-Speed CMOS Lo Design, c) Transfer Gate and Dynamic Logic Design

Convener(STTP) - Dr.S.S.Shriramwar

Coordinators(STTP) - Dr.Mrs.M.V.Vyawahare , Mrs.A.P.Khandait, Ms.D.Meshram

INAUGURAL SESSION :
Program was Inaugrated by Mr.Prathipan K., **Research Scientist, DRDO**, Dr. M.P.Singh, Principal & Dr.S.A.Dhale ,Vice-Principal, PCE
Program started with introduction and welcome of guests by Dr.Mrs. M.V.Vyawahare, Coordinator STTP
Dr.S.S.Shriramwar, Convener & Dean Academics briefed about the objectives of STTP.
Dr.S.A.Dhale,Vice Principal Spoke about the benefits of STTP to the participants.
Mr. Prathipan.K, Chief guest, in his speech focused on VLSI Design and it's Applications
Dr. M. P. Singh, Principal briefed about the achievements of PCE and importance of such STTPs .
Vote of thanks was proposed by Mrs.A.P.Khandait, Coordinator STTP
Program was conducted by Ms.Divya Meshram , Coordinator, STTP
Total 84 participants were selected for the STTP on first come first serve basis.



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4. AICTE STTP on "Recent Trends and Applications on Analog VLSI Design"

REGISTRATION FORM

AICTE Sponsored

One Week Online Short Term Training Program (STTP)

On

Recent Trends & Applications in Analog VLSI Design

26th to 31st October 2020

Registration form Link

https://tinyurl.com/y6owjh42

Name: _____

Designation: _____

Qualification: _____

Department: _____

College/Organization: _____

Contact Address: _____

_____

_____

Mobile Number: _____

E-mail: _____

Date: Signature of Applicant

Name/ Signature of Head of institution

Kindly upload this form on registration link or e-mail on karunabogawar55@gmail.com

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Dr. Satish Chaturvedi ,Chairman, LTJSS, Nagpur.
Smt. Abha Chaturvedi, Secretary, LTJSS, Nagpur.

Patrons

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Smt. Sheetal Chaturvedi, Member (GB), LTJSS,Nagpur
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STTP Chairperson

Dr. M.P. Singh, Principal, PCE

Advisory Board

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Dr.K.S. Zakiuddin ,Asso. Dean (R&D)
Dr.P.R.Rothe. Dean, SW&C, PCE
Dr.Mrs. S.W.Varade, Professor,Dept of E&T
Dr. V.K.Taksande, HOD Dept of E&T.

Convener

Dr.S.S.Shriramwar, Professor & Dean Academics

Coordinators

Prof. (Mrs.)K.M.Bogawar
Prof. (Ms.) S.G.Mungale

Organising Committee

Prof. (Mrs.) P.J.Suryawanshi
Prof.(Mrs.) A.P.Khandait
Prof. C.N.Bhoyar
Dr. (Mrs.) M.V Vyawahare
Prof.(Mrs.) D.D.Shende
Dr.(Mrs).A.S.Khobragade
Prof. R.C. Iyer

Lokmanya Tilak Jankalyan Shikshan Sanstha's
PRIYADARSHINI COLLEGE OF ENGINEERING
NAGPUR (MAHARASHTRA)

AICTE Sponsored

One Week Online Short Term Training Program (STTP)

On

Recent Trends & Applications in Analog VLSI Design

26th to 31st October 2020

ORGANIZED BY

Internal Quality Assurance Cell

&

Department of Electronics Engineering

Priyadarshini College of Engineering

Priyadarshini Campus, Hingna Road Nagpur-440019
07104-244681
www.pcenagpur.edu.in
Affiliated to RTM Nagpur University
NAAC Accredited with A+ grade
Platinum Category in AICTE-CII Survey

Lokmanya Tilak Jankalyan Shikshan Sanstha's

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(Recognised by A.I.C.T.E., New Delhi & Govt. of Maharashtra, Affiliated to R.T.M.Nagpur University)

Near CRPF Campus, Hingna Road, Nagpur-440 019, Maharashtra (India)

Phone : 07104 – 236381, 237307, Fax : 07104 – 237681,

email : principal.pce.ngp@gmail.com, www.pcenagpur.edu.in

About Institute

Priyadarshini College of Engineering, Nagpur the Premier College of the LTJSS Spread over a sprawling 72 acres,the campus is enriched with state of the art sports and recreational facilities. The Institute has a 32 years of Proven Track Record, endeavors to impart academic excellence through promoting technology, scientific thinking and Corporate Social Responsibility. Priyadarshini College of Engineering has been **awarded with A+ grade status with CGPA 3.31 by NAAC** for a term of 5 years up to 27.03.2024.The **institute has received accreditation for three of its programs**, namely Civil Engineering, Mechanical Engineering, and Electrical Engineering up to 30/06/2021 by **National Board of Accreditation (NBA)**, New Delhi. The Institute runs **7 undergraduate programs, 4 post Graduate Programs and 3 Ph.D. Programs. Institute has a strong faculty pool with 50 Ph.D. awarded and 32 ongoing.** The Institute has also been conferred with **Grade A** by the Government of Maharashtra for Academic Excellence and is the recipient of **Platinum Rank Category in AICTE-CII survey in 2019**.The Institute has also **received World Education Award**, India's Education Excellence Award 2018, Berkshire Media USA; and **Outstanding Engineering Institute** for Research and Innovation held at 15th World Education Summit-2019.

About STTP

Due to the rapid growth and advancement of the Very Large Scale Integration (VLSI), the electronics industries have achieved tremendous growth from last few years. VLSI technology has opened vast opportunities for career growth in design implementations ,verification, computer-aided designing, testing and simulation. So there is a need to produce highly skilled design engineers. The aim of this course is to upgrade the information about the recent trends & applications in design of analog VLSI integrated circuits. Exposure and hands-on training with VLSI Design tools will be part of the course. This STTP also aims to share the experiences of professionals working in the domain of Analog VLSI Design which will help the research scholars and the faculty members to get the in depth knowledge in the field of Analog VLSI design

STTP Objectives

- Recognize the role of analog VLSI design in semiconductor industry & industrial challenges.
- Development of trained resources in VLSI design
- Interaction of the participants with the experts from academic institutes & industry.
- Insights about technological details of VLSI system

Resource Persons

Distinguished faculty members from the renowned Institutes like IIT, NITs, and experts from Industries, and other leading institutions will be delivering the Lectures/demonstrations.

Major Contents

- Introduction to VLSI and Industry Overview
- VLSI Design Flow
- Invited talks delivered by experts is from industry and academic organizations
- Demonstrations through simulations.

Expected Outcomes

- Interaction of the participants with the experts from academic institutes & industry.
- Participants will get acquainted with IC design flow.
- Development of laboratory exercises related to analog VLSI design.
- Manpower development in the area of design of Front End and back end VLSI Design
- Exposure to industry standard toolsets for analog VLSI design.

Registration Guidelines

- **Register on following link**
  https://tinyurl.com/y6owjh42
- Seats are limited and selection will be based on first come first serve basis. Kindly register before 22nd October 2020.
- Confirmation email will be sent to the selected candidates.
- e-Certificate will be issued to the participants who attend all sessions of the STTP and pass the Examination.
- **Registration Fees: Nil**

Contact

Prof (Mrs.) K.M.Bogawar :8600437050

Prof.(Ms.) S.G.Mungale : 9970615935

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Recent Trends & Applications in Analog VLSI Design
26th to 31st October 2020

Organized by : Internal Quality Assurance Cell & Department of Electronics Engineering.

Participated by : Research Scholars, Academicians from Electronics background across the country.

Mode of Conduction: Zoom Platform

Date: 26th Oct- 31st Oct 2020

Event: AICTE sponsored One Week Online Short Term Training Program on Recent Trends & Applications in Analog VLSI Design.

Objective: To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in Analog, VLSI system design, and Hardware Software Co-Design.

To provide scope for Applied Research and innovation in the various fields of VLSI.

To explore new development & innovations & possibility of research in the recent trends in VLSI.

Resource Persons:

Day/Date	Time	Speaker	Topic
Day 1 26/10/20 Monday	10:30 to 10:45 am	Inauguration	
	10:30 to 12:00 pm	Dr.Rajendra Patrikar Professor VNIT,Nagpur	Analog VLSI design using MEMS
	12:00 to 1:00 pm	Dr.Surendra Rathod Professor & Head (Electronics Department) SPIT Mumbai	Evolution of Microelectronics & its future trends with respect to Nanometer era

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Day 2 27/10/20 Tuesday	2:00 to 3:00 pm	Dr.Mrs..D.Malathi, Professor (Department of E &T) Kongu Engineering College, Tamilnadu	Machine Learning using VLSI
	3:00 to 5:00 pm	Mr.L.V.Kedharnath Field Application Engineer, Entuple Technologies Pvt.Ltd.	Full Custom IC Design flow using Cadence
Day 3 28/10/20 Wednesday	2:00 to 3:00 pm	Dr.Mrs.Prachi Palsodkar Asst. Professor, YCCE Nagpur	Challenges in Analog CMOS VLSI Design
	3:00 to 5:00 pm	Mr. L.V.Kedharnath Field Application Engineer, Entuple Technologies Pvt.Ltd.	Semi-Custom IC Design flow using Cadence
Day 4 29/10/20 Thursday	2:00 to 4:00 pm	Dr.Pravin Zode Asstt. Professor Department of E&T,YCCE ,Nagpur	Analog VLSI Design using SPICE
	4:00 to 5:00 pm	Shrutika Solat RF Design Engineer SM Technologies Pvt.Ltd	Introduction & Application of Voltage amplifier IC & design using EDA tool
Day 5 30/10/20 Friday	2:00 to 3:00 pm	Dr.Ketan Raut Asst. Professor VIIT Pune	Recent Trends in Low Voltage analog IC Design
	3:00 to 4:00 pm	Dr.P.R.Rothe Dean SW &C, PCE,Nagpur	DSP Based Analog and Mixed Signal Testing
	4:00 to 5:00	Shrutika Solat RF Design Engineer SM Technologies Pvt.Ltd	Introduction & Application of Power Divider IC & design using EDA tool
Day 6 31/10/20 Saturday	2:00 to 3:00 pm	Mr. Vaibhav Pavnaskar Design Engineer, Microchip, Ireland	Recent Trends in analog RF IC Design
	3:00 to 4:00 pm	Dr.Mrs..D.Malathi, Professor (Department of E &T) Kongu Engineering College, Tamilnadu	VLSI Signal Processing
	4.00 pm	Valedictory Function	

Coordinators:

Dr.M.P.Singh	Chairperson
Dr.S.S.Shriramwar	Convener STTP, IQAC Coordinator
Ms.S.G.Mungale	Coordinator-STTP
Mrs.K.M.Bogawar	Coordinator-STTP

Remark: Participants were enriched with the knowledge shared by expert speakers to keep pace with the changing scenario in the field of Analog VLSI Domain.

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Report on STTP

AICTE sponsored

Online One Week Short Term Training Program on Recent Trends & Applications in Analog VLSI Design

Day-1

Date: 26/10/2020

Program was inaugurated by Dr. R. M. Patrikar Professor VNIT,Nagpur, Dr. M.P.Singh, Principal & Dr.S.A.Dhale ,Vice-Principal, PCE

Program started with introduction and welcome of guests by Mrs.K.M.Bogawar, Coordinator STTP

Dr.S.S.Shriramwar, Convener & IQAC coordinator briefed about the objectives of STTP.

Dr.S.A.Dhale,Vice Principal spoke about the benefits of STTP to the participants.

Dr. R.M. Patrikar, Chief guest, in his speech focused on Recent Trends in VLSI Design.

Dr. M. P. Singh, Principal * briefed about the achievements of PCE , extended best wishes and Congratulated the STTP team for their efforts.

Vote of thanks was proposed by Ms.S.G.Mungale, Coordinator STTP

Two sessions were delivered today .

Session-1: Dr. R. M. Patrikar Professor VNIT,Nagpur delivered expert talk on " Analog Design using MEMS".

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Date: 31/10/20

Session 1- Mr.Vaibhav Pavnaskar , Design Engineer Microchip, Ireland delivered expert talk on Recent Trends in Analog RF IC Design .

Session-2: Dr. D. Malathi, Prof. Kongu Engg.College , Erode, TN delivered expert talk on " VLSI Signal Processing".

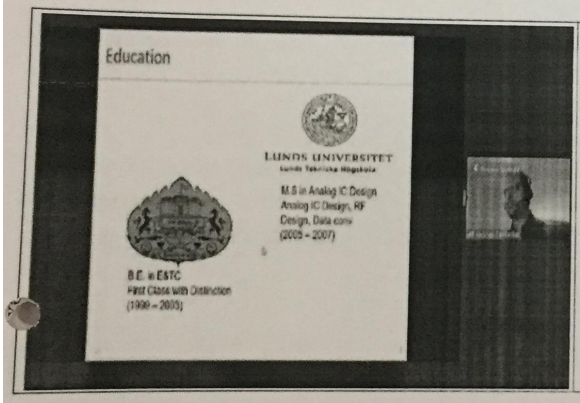
The STTP ended with the valedictory function in presence of Dr.M.P.Singh, Principal,PCE,Nagpur. Total 18 sessions were delivered by 11 experts from Academia and Industry and one International expert from Ireland.

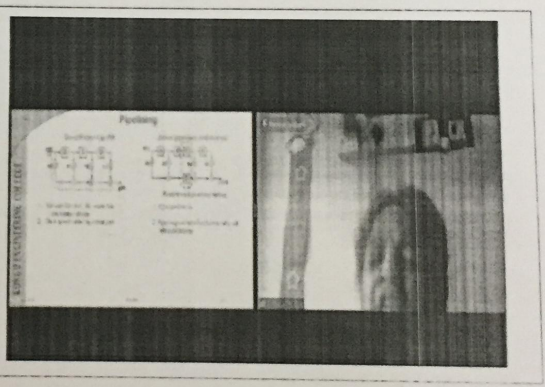
Feedback on STTP was taken from the participants and received very good feedback.

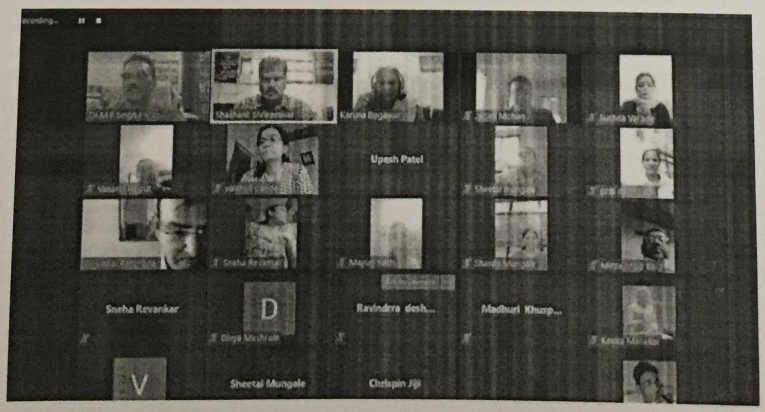
Summary Report of STTP was presented by Ms.S.G.Mungale

Mrs. K.M.Bogawar proposed vote of thanks

Dr. M. P. Singh Principal Congratulated the the organizing team for successful completion of STTP.







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5. A one day workshop on "NAAC SSR and Documentation", 30/09/2020